AMENDMENTS TO THE SPECIFICATION

Amend the abstract as follows:

[0049] Disclosed herein is an improved serializer/deserializer (SERDES) circuit (102) having built-in self-test capabilities that is configured to perform an in-situ jitter sensitivity characterization of the clock and data recovery (CDR) circuit (108). To that end, a delay perturbation is added to the serial data stream at the serializer (120) output, typically using a variable delay (DEL) line (116). Then, the perturbed serial data stream is looped back to the CDR circuit. A dedicated circuit in the control logic (112) coupled to the DEL line and the deserializer circuit (110) analyzes the recovered data to characterize the sensitivity of the CDR circuit to the jitter frequency. By continuously modifying the output delay of said serial data stream, i.e. the amplitude and the frequency of the perturbation, one can generate a perturbed serial data stream, very close to the real jittered data. ~~Moreover, the perturbed data stream can be transmitted to any distant SERDES circuit (104) before it is looped back to the CDR circuit. By comparing the jitter sensitivity with and without using the transmission link (106), one can easily characterize the amount of jitter added by said link. A method of testing the jitter sensitivity of the CDR circuit is also disclosed.~~